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HARRY A WOLIN
MOTOROLA INC
AUSTIN INTELLECTUAL PROPERTY LAW SEC
7700 WEST PARMER LANE MD TX32 PL02
AUSTIN, TX 78729

EXAMINER
ESTRADA, MICHELLE

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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Paper No. 25

Application Number: 09/443,443
Filing Date: November 22, 1999
Appellant(s): POZDER ET AL.

Joseph Lally
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed 10/30/02.

(1) Real Party of Interest

A statement identifying the real party of interest is contained in the brief.

(2) Related Appeals and Interferences

A statement identifying the related appeals and interfereces, which will directly affect or be directly affected by or have a bearing on the decision in the pending appeal is contained in the brief.

(3) Status of Claims

The statement of the status of the claims contained in the brief is correct.

(4) Status of Amendments After Final

The statement of the status of the amendment after final is correct.

(5) Summary of Invention

The summary of the invention contained in the brief is correct.

(6) Issues

The appellant's statement of the issues in the brief is correct.

(7) Grouping of Claims

Appellant's brief includes a statement dividing the claims into groups and that the claims of each group stand or fall together and provides reasons as set forth in the Argument.

(8) Claims Appealed

The copy of the appealed claims contained in the Appendix to the brief is correct. A correct copy of the appealed claims is submitted herewith.

(9) References of Record

The following is a listing of the prior art of record relied upon in the rejection of claims under appeal.

5,149,674	Freeman, Jr. et al.	09-1992
5,989,991	Lien	11-1999
4,723,197	Takiar et al.	02-1988
5,942,448	White	08-1999
5,912,510	Hwang et al.	06-1999

(10) Grounds of Rejection

The following grounds of rejection are applicable to the appealed claims:

Claims 1-5, 10, 24-27, 30 and 32 are rejected under 35 U.S.C. 103(a) as being unpatentable over the combination of Freeman, Jr. et al. and Lien.

Freeman, Jr. et al. disclose a method for forming a semiconductor device comprising forming an uppermost interconnect level that includes an interconnect portion which can be made of copper (13) and a bond pad over; forming a passivation layer (19) over the uppermost interconnect level, wherein removing portions of the passivation layer exposes portions of the bond pad (18) and forms a plurality of support structures overlying the uppermost surface of the bond pad; and forming a conductive capping layer (27) which can include aluminum overlying the plurality of support structures, wherein the conductive capping layer electrically contacts the bond pad (Col. 3, line 19- Col. 5, line 14); forming dielectric studs (14) within the bond pad (18) , wherein at least a portion of a support structure overlies a portion of a dielectric stud; wherein the plurality of support structures are interconnected with unremoved portions of the passivation layer. Furthermore, (14) are studs because they have vertical and

lateral extent. The claims do not require the configuration of studs shown in figure 3. The reference also discloses that the bonding pad (10) conducts electrical signals into and out of the integrated circuit located on the remainder of the semiconductor substrate (Col. 2, lines 15-18); wherein (19) is silicon oxide or any other suitable material (Col 3, lines 52-58).

Freeman, Jr. et al. do not disclose forming a first interconnect level over a semiconductor substrate; wherein the first interconnect level includes that the interconnect portion contacts the first interconnect level by way of vias through an interlevel dielectric layer, and wherein all vias interconnecting the interconnect portion and the first interconnect level are positioned outside regions directly below the bond pad.

Lien discloses forming a first interconnect level (210) over a semiconductor substrate; forming a bonding pad (216); wherein the first interconnect level includes that the interconnect portion contacts the first interconnect level by way of vias through an interlevel dielectric layer (206/207/208), and wherein all vias interconnecting the interconnect portion and the first interconnect level are positioned outside regions directly below the bond pad (See fig. 3); wherein the bonding pad is formed near an edge of the integrated circuit (Col. 1, lines 45-46).

It would have been within the scope of one of ordinary skill in the art to combine the teachings of Freeman, Jr. et al. and Lien to achieve formation of interconnects in the bonding pad structure of Freeman, Jr. et al.

Claim 6 are rejected under 35 U.S.C. 103(a) as being unpatentable over the combination of Freeman, Jr. et al. and Lien as applied to claims 1-5, 10 24-27, 30 and 32 above, and further in view of Takiar et al.

The combination of Freeman, Jr. et al. and Lien does not specifically disclose forming the bond pad over a dielectric layer having a Young's modulus less than approximately 50 Giga Pascals or having a low yield strength.

Takiar et al. teach a method of forming a conductive bond pad including forming the bond pad over dielectric layers including silicon nitride, silicon oxynitride, polyimide, silicon nitride, and silicon dioxide (Col. 2, line 53- Col. 3, line 34). These materials are considered preferred materials in the instant application.

It would have been within the scope of one with ordinary skill in the art at the time of the invention to combine the teachings of Freeman, Jr. et al., Lien and Takiar et al. to enable formation of the bond pad over the recited dielectric layers.

Claims 8, 9, 28-29 and 31 are rejected under 35 U.S.C. 103(a) as being unpatentable over the combination of Freeman, Jr. et al. and Lien as applied to claims 1-5, 10 24-27, 30 and 32 above, and further in view of White.

The combination of Freeman, Jr. et al. and Lien does not disclose forming a barrier layer, which includes a material, selected from the group consisting of tantalum, titanium, tungsten, and chromium between the capping layer (27) and the conductive bond pad (13).

White teaches forming a conductive bond pad (22) with a capping layer (26) with a barrier layer (24) disposed there between. (24) is made of titanium-tungsten.

It would have been within the scope of one with ordinary skill in the art at the time of the invention to combine the teachings of Freeman, Jr. et al., Lien and White to enable formation of the bond pad and capping layer of the combination to be performed.

Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over the combination of Freeman, Jr. et al. and Lien as applied to claims 1-5, 10 24-27, 30 and 32 above, and further in view of Hwang et al.

The combination of Freeman, Jr. et al. and Lien does not disclose forming the conductive capping layer (27) from a material selected from the group consisting of nickel and palladium.

Hwang et al. teach the suitability of using nickel to form a capping layer over a bond pad. (Col. 3, lines 8-25 and Fig. 2).

It would have been within the scope of one with ordinary skill in the art to combine the teachings of Freeman, Jr. et al., Lien and Hwang et al. to enable formation of the capping layer of the combination.

(11) Response to Argument

Appellant argues that Freeman and Lien both teach conventional patterning of the passivation layer in which a single, large opening is formed over the bond pad, in Freeman the passivation layer 28 is patterned to form a single opening exposing the

underlying interconnect while in Lien the passivation layer 209 is likewise patterned to form a single, conventional opening over the bond pad. However, the Freeman, Jr. et al. discloses forming plural openings in passivation layer 19 to expose bond pad 18.

Appellant argues that the perforated interlevel dielectric of Freeman does not suggest a perforated passivation layer as recited by Appellants because the purpose of perforating the dielectric layer in Freeman us to achieve greater planarity in a multi-layer bond pad structure. It appears that the language in question is in claim 1, lines 11-14, for example. However, it is not necessary that Freeman discloses the same advantages as the instant invention; it is sufficient that the same materials are treated in the same manner. The reference discloses patterning the passivation layer 19 as recited (Col. 4, lines 37-39).

Appellant argues that the perforated passivation layer in Freeman or Lien would have a serious technical drawback in that it would reduce the size of the "probable" area of the bond pad and lead to possible discontinuities. However, the claims are open to that process.

Appellant argues that neither Freeman or Lien disclose any deposition of a conductive capping layer over the perforated bond pad. However, Freeman discloses depositing a conductive capping layer (27) over the perforated passivation layer (Col. 5, lines 1-2).

Appellant argues that in Freeman, the structure that would correspond to the support structure of Appellants' is a free-floating structure that is not connected to the un-removed portions of the corresponding dielectric layer, and that Freeman is not

directed to providing mechanical support and protecting against probe forces. However, appellant has not provided a convincing argument that the term requires the remaining portions of the dielectric to be connected. Those structures would provide support as recited. The structure of Freeman is encompassed by the term as recited.

Appellant argues that neither Freeman nor Lien discloses a multi-layer bond pad. However, neither Freeman nor Lien was relied on upon for that purpose. White is relied on to disclose the multi-layer bond pad.

Appellant argues that since aluminum is a self-passivating metal, there is no need to cap the aluminum with another material because aluminum suffices as an upper, exposed layer for the bond pad structure. However, it would have been obvious to cap the aluminum with another material because it will perform many functions such as retarding the diffusion of material between the bond pad and the bump, and providing a voltage potential during the electroplating process to follow as disclosed in White (Col. 3, lines 20-23).

For the above reasons, it is requested that the honorable Board of Patent Appeals and Interferences sustain the rejections above.

Respectfully submitted,

MEstrada
January 8, 2003

Conference:

Olik Chaudhuri
Supervisory Patent Examiner
Art Unit 2823

Wael Fahmy
Supervisory Patent Examiner
Art Unit 2814

Michelle Estrada
Examiner
Art Unit 2823